Panoptic Dynamic Voltage Scaling for Low Power Design

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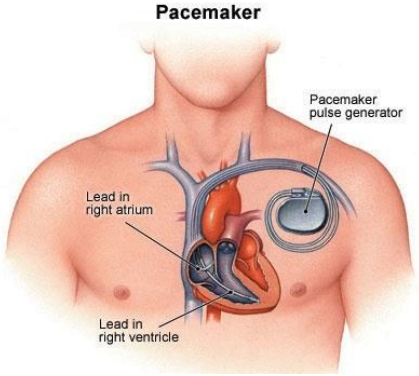
Outline

- Motivation
- Current Architectures
- Panoptic Dynamic Voltage Scaling (PDVS)
- Benefits/Overheads of PDVS
- Variable Weighted Headers as a LDO
- Benefits/Overheads of LDO Approach

Motivation

- Portable applications require extended battery life & small form factor
- Don’t sacrifice performance when required
- Electronics need high performance for a fraction of their life



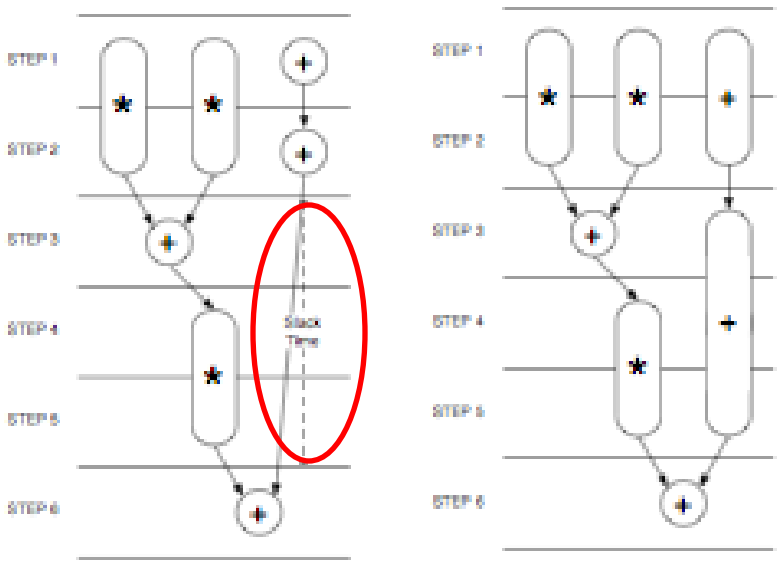
Dynamic Voltage Scaling (DVS)

When possible, switch down to lower V_{DD} to save energy but still meet performance requirements

$$E = C * V_{DD}^2$$

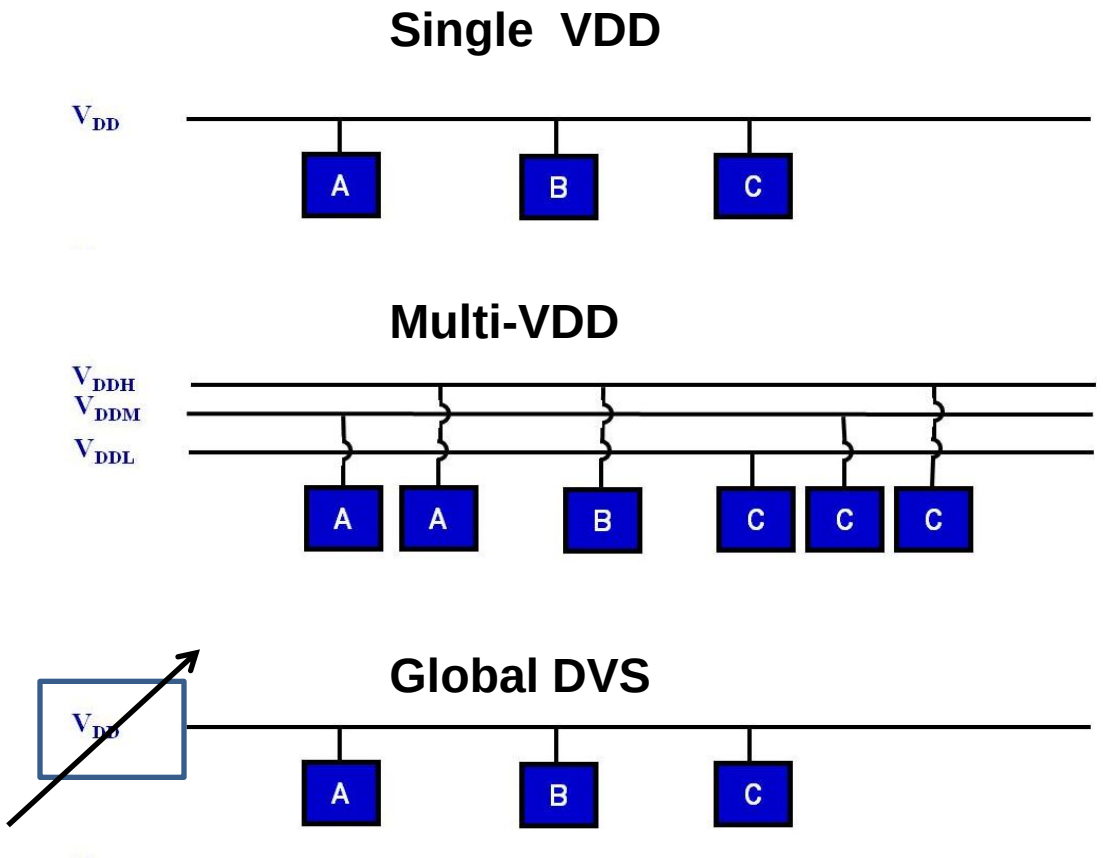
$$\tau = RC = \frac{V_{DD}}{I} C$$

Trade energy for delay.



Timing Slack Inherent in Benchmarks

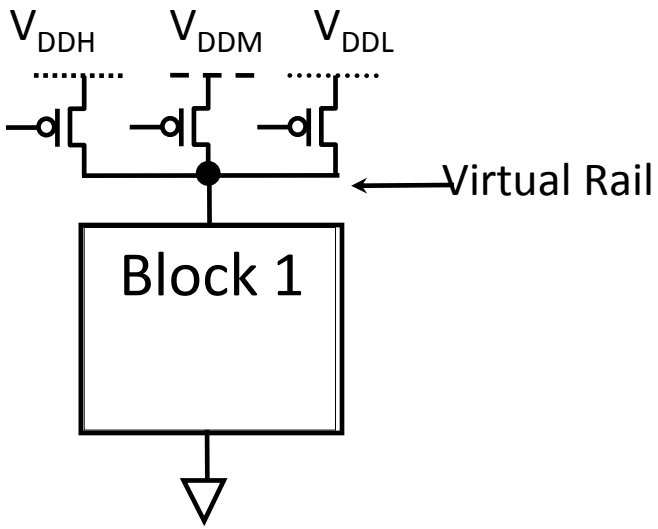
Current Architectures



A B C blocks can be adders/multipliers or cores/multiple cores

Panoptic Dynamic Voltage Scaling

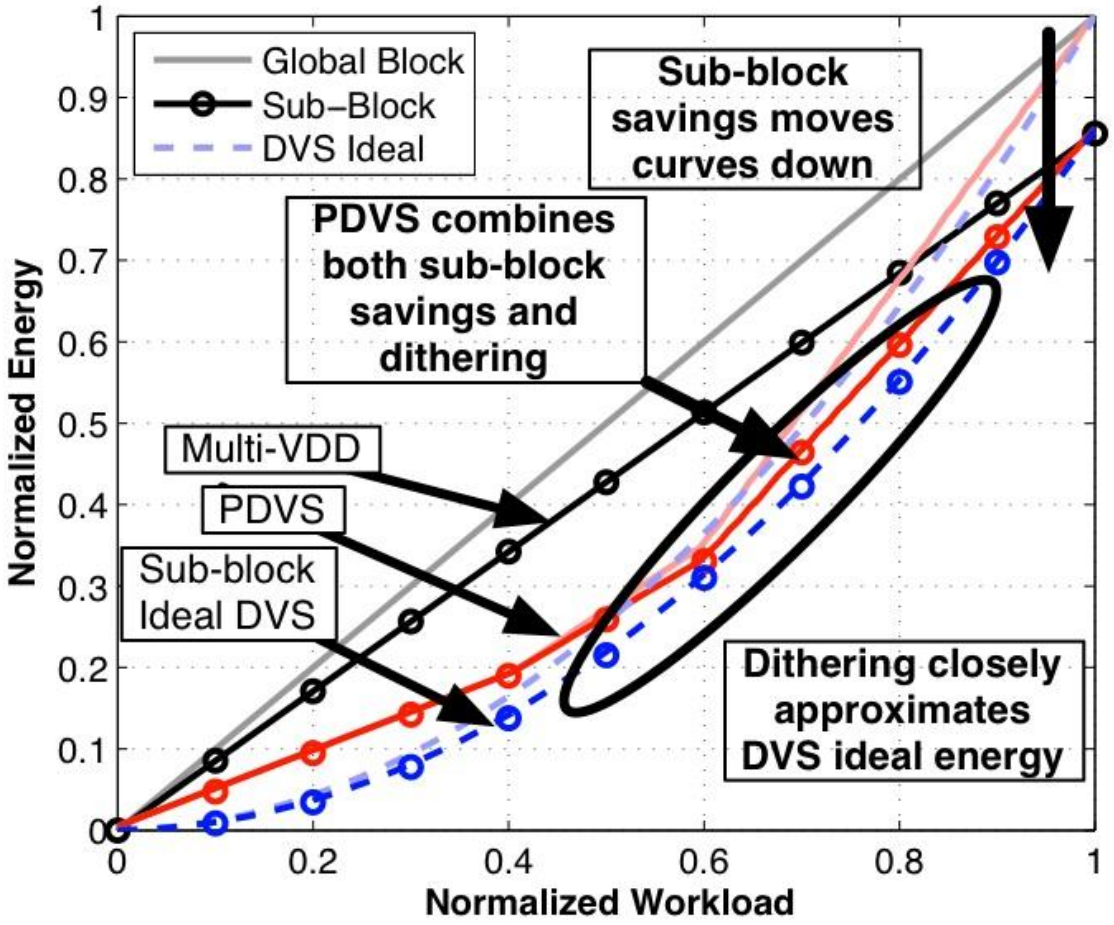
- 3 rails distributed throughout the chip
- Headers (PMOS transistors) connect block to voltage supply
- Sub blocks (adders/multiplier) can connect to an rail
- Voltage assigned to operation
- Single clock cycle V_{DD}-switching at the component level
- Allows trade of delay and speed.
- Assign operation to voltage, not component to voltage



PDVS Benefits

- Reduction in DC-DC converter time/energy (no switching like other DVS Scheme)
- **Spatial Granularity** - ability to assign each component to different voltages at any given time
- **Temporal Granularity** - ability to adjust a component's voltage quickly
- Area savings over Multi-VDD

Benchmark Savings



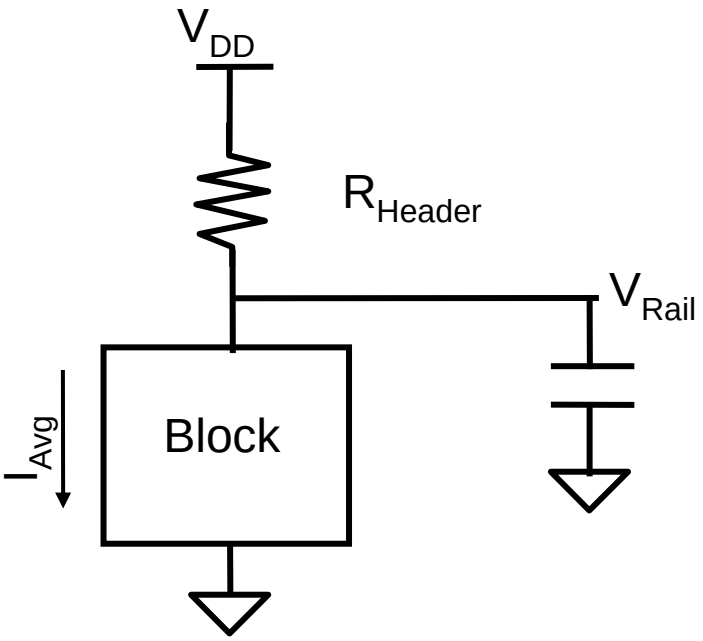
Voltage dithering- operating at higher voltage and then lower voltage to avg performance to achieve any effective performance rate in between.

Overheads of PDVS

- Rail recovery energy

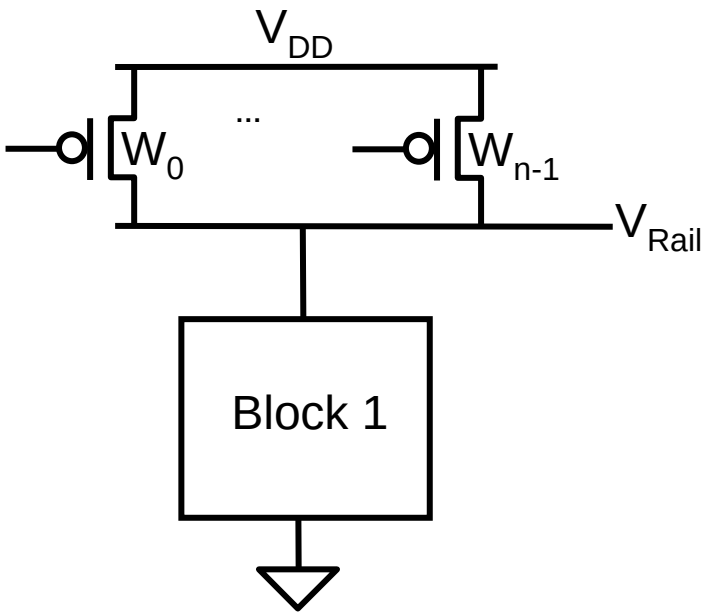
$$E_{rec} = C_{block} V_{DD} (V_{DD} - V_{rail})$$

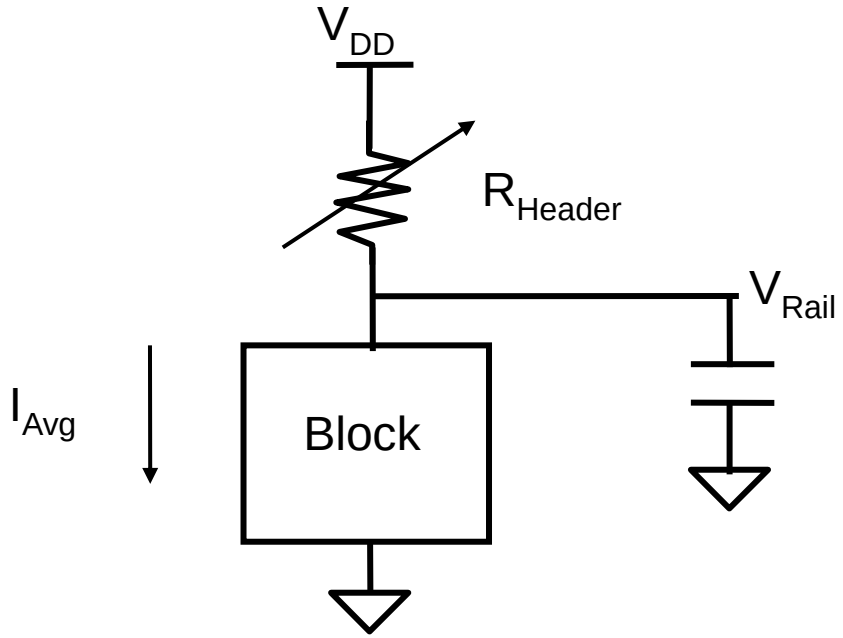
- Extra metal routing
- Complexity (more control signals)
- Delay, energy, and area of level converters to reduce static current
- Delay, energy, and area of headers



Variable Weighted Headers

We can utilize the existing header infrastructure to provide more energy savings opportunities.

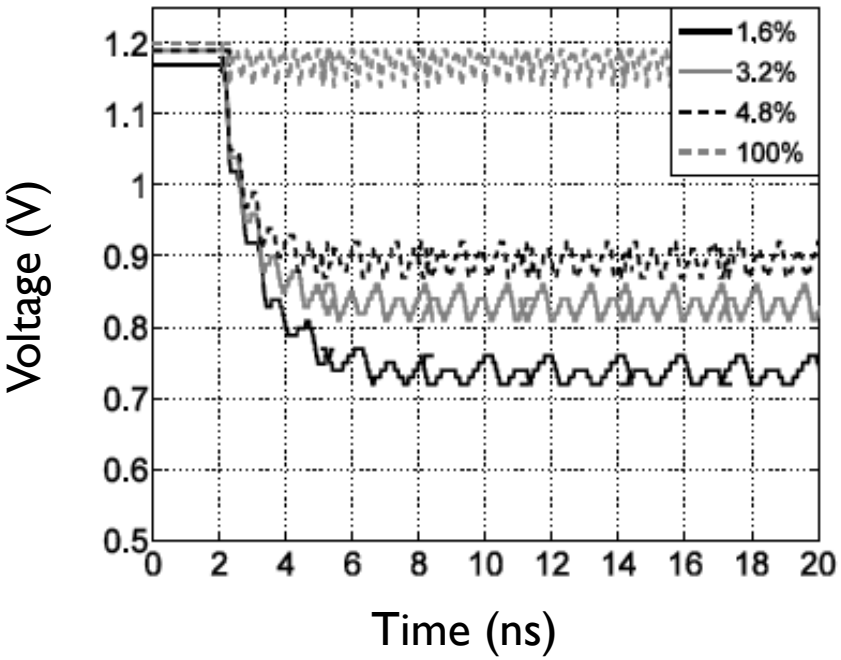




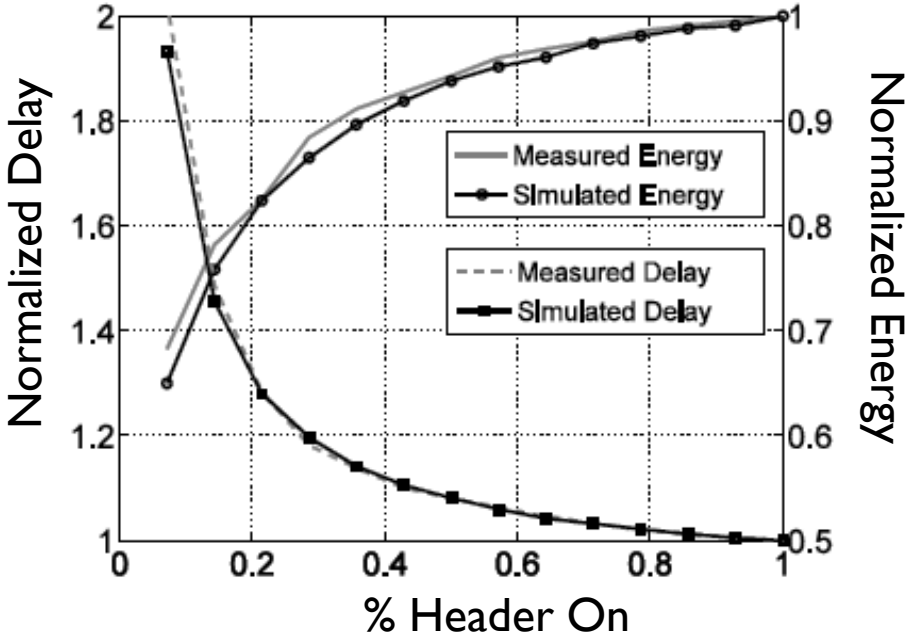
Split up the header into individually controllable parallel transistors

Based on # of headers on, we can control resistance/Vrail

Low Dropout Regulator (LDO)



Virtual rail of a 32b Kogge Stone adder during successive adder operations over several header widths.



Simulated and measured energy & delay for a ring oscillator with sweeping header size.

LDO

Benefits

- More voltage possibilities without more DC-DC converters
- Energy savings

$$E_{op} = C_{block} V_{DD} V_{rail} \quad (1)$$

$$E_{op} = C_{block} V_{rail}^2 \quad (2)$$

Overheads

- Recovery Energy

  $$E_{rec} = C_{block} V_{DD} (V_{DD} - V_{rail})$$

- Increased number of wires → Increased cap → Increase gate switching energy
- Complexity

Conclusions

PDVS can be used to extend battery life by leveraging variable work rate and existing slack.

PDVS's (and powergating's) headers can be used as LDO to save energy.

Questions?

Benefits of the LDO Approach

- Reduction in DC-DC Converters
- Finer granularity
- Energy savings

$$E_{op} = C_{block} V_{DD} V_{rail} \quad (1)$$

$$E_{op} = C_{block} V_{rail}^2 \quad (2)$$

$$E_{op} = C_{block} V_{rail}^2 + (V_{DD} - V_{rail}) I_{avg} \quad (3)$$